

# TRANSMISSION LINE PARASITIC ELEMENT DISCONTINUITY CANCELLATION

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## CLAIM OF PRIORITY

The present application claims the benefit of and incorporates by reference U.S. Provisional Application Serial No. 60/239,020, filed October 4, 2000. This is a continuation of copending application number 09/970,550 filed on October 3, 2001,  
10 which is hereby incorporated by reference herein.

## BACKGROUND

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Buses are commonly used in computers and other electronic devices to send signals containing data from a driving (or generation) point to any number of receiving points. These busses can be created in printed circuit technology or from cables attached from one point to a second point. Backplane buses use circuit cards that plug in at regular intervals and represent loads along the bus. Cable busses employ cables with  
20 uniform electrical parameters that are connected at load devices in, for example, a daisy-chain fashion. Such a connection is used, for example, in Small Computers Systems Interface (SCSI) implementations.

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The SCSI type of bus is also adaptable for use within backplane architectures. In systems of this type, the cable bus is replaced with a printed circuit board backplane. Intelligent peripheral devices, in the form of daughter boards, are then connected to the backplane connectors. The backplane architecture provides a compact and efficient method for connecting a series of intelligent peripheral devices to a computer system.

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To work properly, a bus must maintain certain electrical characteristics. One of

these characteristics is a controlled impedance. For an unloaded bus (i.e., a bus with no attached intelligent peripheral devices), the intrinsic impedance ( $Z_{sub.0}$ ) can be calculated using the intrinsic impedance per unit length ( $L_{sub.0}$ ) and the intrinsic capacitance per unit length ( $C_{sub.0}$ ) in the following equation:

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$$Z_{sub.0} = (L_{sub.0} / C_{sub.0})^{1/2}$$

For a loaded bus, the preceding equation must be modified to reflect the effect of the attached load devices. This is most always in the form of added capacitance attributable to the attached load devices. Specifically, for a loaded bus the impedance ( $Z'$ ) can be calculated by modifying the preceding equation to include the load capacitance per unit length ( $C_{sub.d}$ ) resulting in the following equation:

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$$Z' = (L_{sub.0} / (C_{sub.0} + C_{sub.d}))^{1/2}$$

Based on this equation, it may be appreciated that increasing the load capacitance per unit length ( $C_{sub.d}$ ) will result in decreasing values for the loaded impedance ( $Z'$ ). Unfortunately, in backplane architectures, the buses are relatively short with each load device being separated by a relatively short distance. Since each load device adds capacitance to the bus, there is a tendency for backplane architectures to have relatively high values for load capacitance per unit length ( $C_{sub.d}$ ). The result is that these architectures may be characterized by low intrinsic low values for impedance ( $Z'$ ). Low values for impedance ( $Z'$ ) results in a slow propagation speed for signals within the bus. This degrades the performance of the bus, making it more prone to operational errors and electrical noise.

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To overcome the degrading effects of decreasing impedance, designers have been faced with a difficult compromise. One possible solution is to increase the length of the bus included in backplane architectures. Typically this is achieved by increasing the

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effective distance that each signal must travel between adjacent intelligent peripheral devices. Unfortunately, this requires that the size of the backplane be increased or that each signal path be routed in a tortuous pattern between adjacent load devices. The use of a tortuous pattern increases the difficulty of routing the signal paths within the backplane and may require that additional signals layers be added to the backplane. In either case, the cost of the backplane can be increased significantly. Another possible solution is to decrease the clock speed of the bus. Of course, this negatively impacts the performance of the bus, thereby making this solution generally unacceptable.

In addition to the problems discussed above, using RAMBUS technology, current computer data speeds may operate at 800 mega-transfers per second. As a result, the edge rates of the data pulses are on the order of 200 picoseconds or 0.2 nanoseconds. For high speed data ASIC comparisons distortions may occur due to reflections of the data signal from the terminating end of the data signal path. This path may include the path through the silicon itself. Further the silicon path also has parasitic load that must be dealt with.

At these very high speeds (edge rates) the effect of otherwise small reactive components attached to electrical interconnects can have a very detrimental effect. The high speed edge rates of the Rambus-generated signals (e.g., in the Alpha EV7 that uses Rambus signals extensively) would cause significant signal reflections off of parasitic load points such as PWB routing vias or connector pins. Also, the transmission line electrical discontinuities caused by these physical discontinuities (like vias and connector pin metallization) would cause a noise margin reduction of these signals and possible logical failures.

Therefore there is now a need for a high speed bus or signal transmission line that has acceptable electrical signal impedance characteristics and operates at acceptable clock speeds.

## SUMMARY

The embodiments of the present invention address the aforementioned and related problems that are associated with a parasitic element. Since a discontinuity, such as a  
5 via, in a signal transmission line can introduce the parasitic element which affects the signal transmission, embodiments of the present invention provides a method and system directed to counteracting that transmission line parasitic element discontinuity.

More specifically, as embodied and broadly described herein, the system includes  
10 signal transmission line and a correction transmission line. The correction transmission line includes, based on the characteristics of the parasitic element, an inductance or a capacitance. The correction transmission line is positioned in the signal transmission line before or after the parasitic element.

15 In further accordance, as embodied and broadly described herein, one method includes determining a value of a parasitic element, be it a capacitive or an inductive parasitic element, that exists at a portion of a signal transmission line which has an impedance. This method also includes calculating a delay associated with a correction  
20 impedance of a correction transmission line that, based at least in part on the parasitic element value and the correction impedance of the correction transmission line, is operative to increase the signal transmission line impedance if the parasitic element is capacitive and to decrease the signal transmission line impedance if the parasitic element is inductive. This method further includes adding the correction transmission line to the  
25 portion of the signal transmission line at which the parasitic element exists.

25 In accordance with this method, the correction transmission line is divided equally and each half-part thereof is applied to the signal transmission line. Moreover, the half-parts of the correction transmission line are added one before and one after the parasitic  
30 element.

In another embodiment, a method enhances signal transmission characteristics of a signal transmission line. This method includes determining an intrinsic capacitance (or inductance) of a parasitic element that exists at a discontinuity portion of a signal transmission line which has an impedance. This method further includes calculating a delay associated with a correction impedance that, based at least in part on the intrinsic capacitance (or inductance) and the correction impedance, is operative to increase the signal transmission line impedance (or decrease the signal transmission line impedance if it is an intrinsic inductance of the parasitic element). Furthermore, this method includes adding the correction impedance to the signal transmission line so that one half of the calculated delay is added before and the other half of the calculated delay is added after the portion of the signal transmission line at which the parasitic element exists.

An advantage of a representative embodiment of the present invention is that it can eliminate the negative affects of parasitic element discontinuity within an electrical system.

Another advantage of a representative embodiment of the present invention is that it provides for the precise calculation of operating characteristics that are affected by capacitance cancellation.

Yet another advantage of a representative embodiment of the present invention is that it controls the impedance and cross talk levels in the ASCI design and incorporates features that cancel out the negative effects of the input capacitance of the silicon die.

Other advantages a representative embodiment of the present invention are that it enhances the manufacturing of electrical systems, is cost efficient, and is easy to implement.

Further advantages of embodiments of the present invention will be understood by those skilled in the art from the description herein. The advantages the embodiments

of the invention will also be realized and attained from practice of the invention disclosed herein.

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## BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and related advantages and features of the present invention will become apparent upon reviewing the following detailed description of embodiments of the invention, taken in conjunction with the following drawings, where like numerals represent like elements, in which:

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FIG. 1 illustrates correcting the transmission line in order to compensate for parasitic capacitance.

FIG. 2 illustrates correcting the transmission line in order to compensate for parasitic inductance.

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FIG. 3 shows the signal paths as determined in accordance with the method of an embodiment of the present invention.

FIG. 4 shows a detailed view of the signal paths as determined in accordance with the method of the embodiment of the present invention.

FIG. 5 shows another detailed view of the signal paths as determined in accordance with the method of the embodiment of the present invention.

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FIG. 6 shows another detailed view of the signal paths as determined in accordance with the method of the embodiment of the present invention.

FIG. 7 shows another detailed view of the signal paths as determined in accordance with the method of the embodiment of the present invention.

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## DETAILED DESCRIPTION

Embodiments of the present invention will now be described with reference to Figures 1-7. This detailed description is provided for the purposed of illustration and

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description. Although the present invention is described with respect to a specific embodiment, various changes and modifications may be suggested to persons of ordinary skill in the art, and it is intended that the present invention encompass such changes and modifications as they fall within the scope of the claims appended hereto.

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Embodiments of the present invention allow for a cancellation (correction) of parasitic elements on a signal transmission line, be they capacitive or inductive, by the use of a length of "correcting" transmission line with a propagation time  $T_c$ . The correcting transmission line will have a characteristic impedance, for example  $Z_c$ , and  
10 an intrinsic propagation delay per unit length of  $D_c$  (i.e., picoseconds per inch). The parasitic element to be cancelled out or counteracted could be a parallel connected capacitance  $C_p$  (such as a stub connected PWB via) or a series connected inductance  $L_s$  (such as a series connected PWB via connector pin). The nominal impedance of the signal transmission line is  $Z_o$  with a nominal delay of  $D_o$ . Embodiments of the invention  
15 allow for a general mathematical solution to calculate the exact amount of transmission line propagation delay of a correcting transmission line to cancel out the impedance discontinuity caused by the reactive parasitic element.

For the correction of a parallel connected parasitic capacitive load the correcting  
20 transmission line impedance ( $Z_c$ ) will need to be higher than the normal impedance in the circuit ( $Z_o$ ) and of a delay  $T_c = (Z_c * C_p) / ((Z_c / Z_o)^2 - 1)$ . For the correction of a parasitic series inductance, the correcting impedance  $Z_c$  will need to be lower than the normal impedance in the circuit and of a delay  $T_c = (L_s / Z_c) / ((Z_o / Z_c)^2 - 1)$ . When applied properly, the impedance  $Z_c$  is "loaded down" to  $Z_o$  by a parasitic capacitance  $C_p$ ,  
25 or  $Z_c$  is "raised up" to  $Z_o$  by the parasitic inductance  $L_s$ . The control of the impedance mismatch comes at a price. There is a known time delay introduced by the correcting transmission line. This will be the value of  $T_c$  (the intrinsic unloaded delay of the  $Z_c$  transmission media) times the ratio of  $Z_c / Z_o$  for capacitive parasitic cancellation or  $T_c$  times the ratio of  $Z_o / Z_c$  for inductive parasitic cancellation. This non-intrinsic delay  
30 penalty shall be called  $T_c'$ . For high frequency applications (fast edge rates) the value of

$Z_c$  should not be close to  $Z_o$  to minimize the value of  $T_c'$  which should not exceed one-half the edge rate of the signal involved if parasitic cancellation is to be effective.

5 The correcting transmission line of impedance  $Z_c$  and delay  $D_c$  could be any conveniently allowed transmission line impedance, speed, and form factor (coaxial, twisted, etc.). The general application can be created on a printed wiring board by etching the correcting transmission line at the same time that the normal signal impedance  $Z_o$  is being etched. This will result in both transmission lines having the same propagation velocity (or unit delay  $D_o$ ), and there will be no additional time or cost  
10 involved. Higher impedances for  $Z_c$  for capacitive parasitic cancellation can be traces etched narrower than the nominal impedance  $Z_o$  and lower impedances for  $Z_c$  can be etched wider than the nominal traces. The preferred implementation divides the calculated time of  $T_c$ , for the chosen impedance  $Z_c$ , into two halves. Each half of  $T_c$  is placed on either side of the parallel capacitance of the series inductance.

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With respect to Figure 1, it can be seen that the signal path is narrower before and after the parasitic capacitance  $C_p$ . The length of each narrow region is  $T_c/2$ . Each of the narrow regions has a chosen impedance  $Z_c$ , while the thick regions of signal path have impedance  $Z_o$ . Using the formulas as discussed above, the dimensions of the signal  
20 transmission path can therefore be customized to eliminate unwanted capacitance. Using conventional integrated circuit package signal transmission path designs, embodiments of the present invention are able to compensate or eliminate up to 2.5 pF of capacitance for a signal with a rise time of 200 picoseconds.

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Figure 2 shows a signal transmission path that has been designed to eliminate a series inductance  $L_s$ . In this example, the necessary chosen impedance  $Z_c$  is less than  $Z_o$  so the signal path is made wider in the region adjacent both sides of the inductor  $L_s$ . Each side of the wide region of signal path is again  $T_c/2$ .

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Figure 3 shows as a solution of an embodiment of the present invention, the

custom routing provided in the ASIC package to provide impedance and cross-talk control. A further feature is to have the signals loop through the package so that it enters, brings the signal to the I/O structure of the die and continues on back out of the package toward the terminator mounted on the surface of the PWB. This allows for compensation on both sides of the load. Figure 3 shows the custom traces required to achieve the nominal Rambus impedance. The wide traces are the Rambus RSL lines and the narrow traces are the "regular" minimum width (35 micron) traces which were used for crosstalk control as well as impedance control. Figures 4-7 show close-up or more precise views of the dimensions of these signal line traces.

At the top of the loop, where the flip chip C4 connections are made, there is a parasitic capacitance caused by the ESD diodes as well as I/O transistor structures. With the given impedance levels of the bus, embodiments of the present invention are able to generate a correction impedance that could cancel out up to 2.5 *pf* of capacitance. For example, the connections were reduced in width to the 35 micron (minimum) for a length of 3.2 mm to cancel out the 1.8 *pf* of parasitic capacitance on-chip.

Figure 4 shows an example of a close up view of the bus signal paths in Figure 3. It can be seen in this example that both the RSL traces and "buddy traces" are 35  $\mu$ m in width. The buddy traces act as electrical shields to intercept any crosstalk between adjacent paths. Any stray signals that enter the buddy traces will therefore be sent to ground and not cause distortion. This greatly enhances the integrity of the signals along the bus lines.

Figure 5 also shows a close up view of some signal paths. In this figure, it can be seen that the RSL traces are 110  $\mu$ m and the buddy traces are 35  $\mu$ m. This embodiment also shows that the spacing between the buddy traces and the RSL lines to be 35  $\mu$ m. It is also shown that the RSL lines change their width from 110  $\mu$ m to 35  $\mu$ m. It is this changing of signal path widths that is in accordance with embodiments of the present invention. As also seen in Figure 4, for a length of 3.2 mm, the signal path just before

entering the chip is reduced in width to 35  $\mu\text{m}$ .

Figure 6 shows signal path CMOS lines that are 35  $\mu\text{m}$  in width with a spacing of 78.1  $\mu\text{m}$  between CMOS lines.

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Figure 7 shows other CMOS signal paths that have adjacent buddy traces. In this area of the bus, the CMOS lines are 35  $\mu\text{m}$  in width with the buddy traces also being 35  $\mu\text{m}$  in width. The spacing is shown at 62.5  $\mu\text{m}$  in this embodiment.

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It is noted that all prior art methods of bus connections do not approach the methods taught by embodiments of the present invention. It is common knowledge that problems with high speed busses existed, however no exact means to compensate for this has been determined until the teachings herein.

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Finally, although the present invention has been described in accordance with the shown embodiments, variations to the embodiments would be apparent to those skilled in the art and those variations would be within the scope and spirit of the present invention. Accordingly, it is intended that the specification and embodiments shown be considered as exemplary only, with a true scope of the invention being indicated by the

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claims that follow and equivalents.